Paper No. 20

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte VATSA SANTHANAM, DAVID GROSS,
and JOHN KWAN

Appeal No. 2001-2302
Application No. 09/002,404

HEARD: December 10, 2002

Before FLEMING, DIXON, and BLANKENSHIP, Administrative Patent Judges.

BLANKENSHIP, Administrative Patent Judge.

DECISION ON APPEAL

This is a decision on appeal under 35 U.S.C. § 134 from the examiner's final rejection of claims 1-4, 7-9, 12, and 15.

We affirm.

BACKGROUND

The invention relates to compiling computer code that pertains to floating-point arithmetic operations. Representative claim 1 is reproduced below.

1. A method for enabling programmatic access to the widest mode floating-point arithmetic supported by a processor, wherein the processor transfers data between memory and its floating-point registers without loss of range or precision, the method comprising the steps of:

(a) defining a floating-point data type having floating-point objects whose memory representations are at least as wide as said floating-point registers;

(b) declaring selected operands of floating-point arithmetic expressions in source code to be of the floating-point data type;

(c) compiling the source code into corresponding object code;

(d) executing the object code; and

(e) performing said floating-point arithmetic, said step (e) including the substep of transferring data between said floating-point registers and memory.

The examiner relies on the following references:

Markstein et al. (Markstein), Wide Format Floating-Point Math Libraries, ACM, 1991, pp. 130-138.[1]

Intel C/C++ and FORTRAN Compilers White Paper (Intel), Intel Corporation, available at http://developer.intel.com/design/perftool/ic124/ic124wht.html (Dec. 11, 1997).

Claims 1-4, 7-9, 12, and 15 stand rejected under 35 U.S.C. § 103 as being unpatentable over Intel and Markstein.

[1] The copy of the reference in the instant file wrapper appears to be a reprint from a paginated journal.

An earlier rejection of claims 7-9 and 15 under 35 U.S.C. § 101 has been withdrawn by the examiner. An earlier rejection of claims 10 and 11 under 35 U.S.C. § 112, second paragraph has been withdrawn after entry of an amendment to claim 10.

Claim 16 has been allowed. Claims 5, 6, 10, 11, 13, and 14 have been objected to as depending from a rejected claim, but deemed drawn to allowable subject matter.

We refer to the Final Rejection (Paper No. 5) and the Examiner's Answer (Paper No. 11) for a statement of the examiner's position and to the Brief (Paper No. 10) and the Reply Brief (Paper No. 12) for appellants' position with respect to the claims which stand rejected.

OPINION

Appellants repeat limitations of the independent claims (Brief at 10), but neither assert that the claims stand or fall separately nor present separate arguments as to why the claims might be thought separately patentable. Accordingly, we select a single claim (claim 1) as representative of the invention. See 37 CFR § 1.192(c)(7).

The examiner bears the initial burden of presenting a prima facie case of unpatentability. If that burden is met, the burden of coming forward with evidence or argument shifts to the applicant. After evidence or argument is submitted by the applicant in response, patentability is determined on the totality of the record, by a preponderance of evidence with due consideration to persuasiveness of argument. In re Oetiker, 977 F.2d 1443, 1445, 24 USPQ2d 1443, 1444 (Fed. Cir. 1992).

In response to the section 103 rejection, appellants argue that Markstein fails to teach or suggest, as set forth by instant claim 1, defining a floating-point data type having floating-point objects whose memory representations are "at least as wide" as the floating-point registers of the associated processor. In particular, appellants submit that the "working precision" (WP) format of floating-point numbers, described by Markstein (p. 130, col. 2) as the "longest format of floating-point numbers supported conveniently by hardware on a computer," does not necessarily correspond to the width of the floating-point registers associated with the processor.

We agree with appellants to the extent there is no express disclosure in Markstein to the effect that the "working precision" width is identical to the width of the floating-point registers of the associated processor. Further, we agree there is insufficient evidence in this record to establish that proposition.

However, a section 103 analysis begins with a key legal question -- what is the invention claimed? Panduit Corp. v. Dennison Mfg. Co., 810 F.2d 1561, 1567, 1 USPQ2d 1593, 1597 (Fed. Cir. 1987). In view of the subject matter embraced by instant claim 1, showing that "working precision" equates with the width of the hardware floating-point registers is not necessary for establishing the case of prima facie obviousness.

Claim 1 recites that the floating-point data type has floating-point objects whose memory representations are "at least as wide" as the floating-point registers of the processor. The claim thus sets a lower limit for width of memory representations

corresponding to the data type -- i.e., the same width as that of the floating-point registers of the processor. However, the language of claim 1 sets forth no upper limit in the range for width of memory representations corresponding to the data type -- the upper extent is based only on the provision that the width is greater than that of the processor's floating-point registers.

We find that Markstein would have suggested floating-point data types (i.e., data types for software implementation of floating-point arithmetic) having floating-point objects with sufficient range and precision such that the width of the memory representations of the objects falls within the unbounded upper range that is claimed by appellants. For example, the reference reports (p. 130, col. 1) that many scientific and engineering calculations required precision greater than the hardware "naturally provided." While we agree that the precision "naturally provided" by the hardware does not necessarily equate with the width of the floating-point registers, Markstein reflects the art-recognized need for precision that may be resolved only by implementation in software. The reference at page 137, first column stresses the need for "a few more bits of precision in certain critical parts" of computations, and suggests the need for manufacturers to provide high performance double precision hardware "as well as an arbitrary floating-point precision facility." That is, Markstein teaches that the need for range and precision in floating-point calculations far exceeds that provided by hardware, and applications requiring great range or precision must rely on software implementations.

Further, Markstein teaches that range and precision much greater than that of "double precision" is indicated for some applications. Appellants provide an example (Brief, ¶ bridging pp. 10 and 11) of hardware floating point registers supporting five decimal place numbers. Appellants submit that "working precision" may represent a format allowing two decimal places, and that "double precision" may allow four decimal places, and such "may also result" in formats smaller than the five-decimal-places hardware floating point registers. Appellants end their example with "double precision," which is far less than the degree of precision taught by Markstein. For example, Markstein speaks of "quad-precision" (p. 130, col. 2), which, using appellants' illustration, would support precision for eight place decimal numbers, as opposed to the five place decimal numbers supported by the hardware floating point registers.

In view of the foregoing considerations, we conclude that the evidence relied upon by the examiner is sufficient to show prima facie obviousness of the invention that is claimed. Burden has shifted for appellants to show that the ultimate conclusion of obviousness is untenable. Appellants have provided no evidence in rebuttal; arguments of counsel are not evidence. See, e.g., Meitzner v. Mindick, 549 F.2d 775, 782, 193 USPQ 17, 22 (CCPA 1977); In re Pearson, 494 F.2d 1399, 1405, 181 USPQ 641, 646 (CCPA 1974).

The arguments submitted in response to the rejection do not persuade us that the section 103 rejection is erroneous. We sustain the rejection of claims 1-4, 7-9, 12, and 15 under 35 U.S.C. § 103 as being unpatentable over Intel and Markstein.

We have considered all of appellants' arguments in making our determinations. Arguments not relied upon are deemed waived. See 37 CFR § 1.192(a) ("Any arguments or authorities not included in the brief will be refused consideration by the Board of Patent Appeals and Interferences, unless good cause is shown.") and §1.192(c)(8)(iv) (the brief must point out the errors in the rejection).

CONCLUSION

The rejection of claims 1-4, 7-9, 12, and 15 under 35 U.S.C. § 103 is affirmed.

No time period for taking any subsequent action in connection with this appeal may be extended under 37 CFR § 1.136(a).

AFFIRMED

MICHAEL R. FLEMING Administrative Patent Judge	)
JOSEPH L. DIXON Administrative Patent Judge	) BOARD OF PATENT) APPEALS) AND) INTERFERENCES
HOWARD B. BLANKENSHIP Administrative Patent Judge	)

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